AMENDMENTS TO THE CLAIMS

1. (CURRENTLY AMENDED) A circuit for converting a first digital signal having a first sample rate to second digital signal having a second sample rate, comprising:

~~a~~ at least two cascaded integration-comb ~~filter~~ filters; and

~~a~~ at least two fractional sample rate ~~converter~~ converters for performing fractional sample rate conversion;

wherein:

a first of said cascaded integrator-comb ~~filter~~ filters and a first of said fractional sample rate ~~converter~~ converters is configured to receive said first signal having said first sample rate and to generate a third digital signal having a third sample rate different from said first and second sample rates; and

a second of said cascaded integrator-comb ~~filter~~ filters and a second of said fractional sample rate ~~converter~~ converters is configured to receive said third signal having said third sample rate and to generate said second signal having said second sample rate.

2. (ORIGINAL) The circuit according to claim 1, wherein said fractional sample rate converter comprises a fractional interpolator.

3. (ORIGINAL) The circuit according to claim 2, wherein said fractional interpolator comprises a numeric controlled oscillator, and a fractional interpolation calculator configured to calculate interpolated sample values based on a timing signal from said numeric controlled oscillator.

4. (ORIGINAL) The circuit according to claim 1, wherein said cascaded integrator-comb filter comprises a differentiation section, an integration section, and a sample-number adjusting section coupled on a signal path between said differentiation section and said integration section.

5. (ORIGINAL) The circuit according to claim 4, wherein said differentiation section comprises N differentiator stages and said integration section comprises N integrator stages, N being an integer greater than zero.

6. (ORIGINAL) The circuit according to claim 1, wherein said third sample rate is intermediate said first sample rate and said second sample rate.

7. (ORIGINAL) The circuit according to claim 1, wherein said third sample rate is closer to a lower of said first

and second sample rates than to a higher of said first and second sample rates.

8. (ORIGINAL) The circuit according to claim 1, wherein said second sample rate is higher than said first sample rate, and said first of said cascaded integrator-comb filter and said fractional sample rate converter is said fractional sample rate converter.

9. (ORIGINAL) The circuit according to claim 1, wherein said first sample rate is higher than said second sample rate, and said first of said cascaded integrator-comb filter and said fractional sample rate converter is said cascaded integrator-comb filter.

10. (ORIGINAL) The circuit according to claim 1, further comprising a band limiting filter coupled between said cascaded integrator-comb filter and said fractional sample rate converter.

11. (ORIGINAL) The circuit according to claim 10, wherein said band limiting filter has a low-pass characteristic for attenuating frequency components higher than about one half of said first sample rate.

12. (ORIGINAL) The circuit according to claim 1, wherein a sample rate conversion ratio of said cascaded integrator-comb filter is an integer ratio.

13. (ORIGINAL) The circuit according to claim 12, wherein said integer ratio is an integer value or 1 divided by an integer value.

14. (ORIGINAL) The circuit according to claim 12, wherein said sample rate conversion ratio of said cascaded integrator-comb filter is greater than 100.

15. (ORIGINAL) The circuit according to claim 1, wherein a first sample rate conversion ratio of said fractional sample rate converter is a non-integer ratio.

16. (ORIGINAL) The circuit according to claim 15, wherein said first sample rate conversion ratio is smaller than a second sample rate conversion ratio of said cascaded integrator-comb filter.

17. (ORIGINAL) The circuit according to claim 1, wherein said first sample rate is less than 100 KHz, and wherein said second sample rate is greater than 10 MHz.

18. (ORIGINAL) The circuit according to claim 1, wherein said circuit is formed in an integrated circuit.

19. (CURRENTLY AMENDED) A method of converting a first digital signal having a first sample rate to a second digital signal having a second sample rate, comprising the steps of:

(A) generating a third signal from said first signal by using a first of a plurality of cascaded integration-comb ~~filter~~ filters and a first of a plurality of fractional sample rate ~~converter~~ converters, said third ~~digital~~ signal having a third sample rate different from said first and second sample rates; and

(B) generating said second signal from said third signal by using a second of said plurality of cascaded integration-comb ~~filter~~ filters and a second of said plurality of said fractional sample rate ~~converter~~ converters.

20. (CURRENTLY AMENDED) A circuit for converting a first digital signal having a first sample rate to a second digital signal having a second sample rate, comprising:

means for generating a third signal from said first signal by using a first ~~of a~~ cascaded integration-comb filter and a first fractional sample rate converter, said third ~~digital~~ signal having a third sample rate different from said first and second sample rates; and

means for generating said second signal from said third signal by using a second ~~of said~~ cascaded integration-comb filter and ~~said~~ a second fractional sample rate converter.